

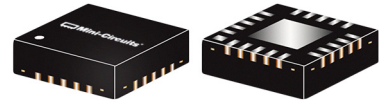
Surface Mount Digital Step Attenuator

DAT-3175A Series

75Ω 0 to 31 dB, 0.5 dB Step 1MHz to 2.5 GHz

The Big Deal

- Wideband, operates up to 2.5 GHz
- Glitchless attenuation transitions
- High IP3, 52 dBm



CASE STYLE: DG983-2

Product Overview

The DAT-3175A+ series of 75Ω digital step attenuators provides adjustable attenuation from 0 to 31 dB in 0.5 dB steps. The control is a 5-bit serial/parallel interface, and the attenuators operate with either single positive or dual (positive and negative) supply voltage. DAT-3175A+ series models are produced by a unique CMOS process on silicon, offering the performance of GaAs with the advantages of conventional CMOS devices.

Key Features

| Feature | Advantages |
|--|---|
| Wideband operation, specified from 1MHz to 2.5 GHz | Can be used in multiple applications such as various versions of DOCSIS, satellite and defense, reducing part count. |
| Serial or parallel interface | Models available with serial or parallel interface mode to suit customer demand. |
| Good VSWR, 1.3:1 typ. | Eases interfacing with adjacent components and results in low amplitude ripple. |
| Single positive supply models: (Model suffixes: -SP+ and -PP+) +2.3 to +3.6V+ | Use of single positive supply simplifies power supply design. An internal negative voltage generator supplies the desired negative voltage. Single positive supply results in excellent spurious performance, -140 dBm typical. |
| Dual supply models: (Model suffixes: -SN+ and -PN+) +2.7 to +3.6V (Positive) and -3.6 to -3.2V (Negative) | Dual supply provides spurious-free operation. It also allows fast switching up to 1 MHz (vs. 25 kHz for single supply). |
| Useable over a wide range of supply voltages, +2.3/2.7 to 5.2V | Wide range of positive operating voltages allows the DAT-3175A+ Series of models to be used in a wide range of applications. See Application Note AN-70-032 for operation above +3.6V |
| Footprint compatible to DAT-3175-XX+ Series (XX=SN/SP/PN/PP) | Can fit into existing footprint and provide wideband performance, to 2.5 GHz instead of 2.0 GHz. |
| Glitchless Attenuation Transitions, 0.26 typical | Compared to previous generation of digital attenuators which is a vast improvement. |



Digital Step Attenuator

75Ω 1-2500 MHz

31 dB, 1.0 dB Step

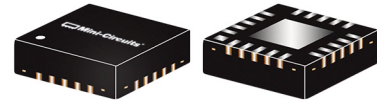
5 Bit, Serial Control Interface, Single Supply Voltage

Product Features

- Single positive supply voltage
- Immune to latch up
- Glitchless attenuation transitions
- Excellent accuracy, 0.1 dB Typ
- Low Insertion Loss
- High IP3, +55-59 dBm Typ
- Very low DC power consumption
- Excellent return loss, 18 dB Typ
- Small size 4.0 x 4.0 mm

Typical Applications

- DOCSIS® 3.1
- Portable Wireless
- CATV & DBS
- MMDS & Wireless LAN
- Wireless Local Loop
- UNII & Hiper LAN
- Power amplifier distortion canceling loops



DAT-3175A-SP+

CASE STYLE: DG983-2

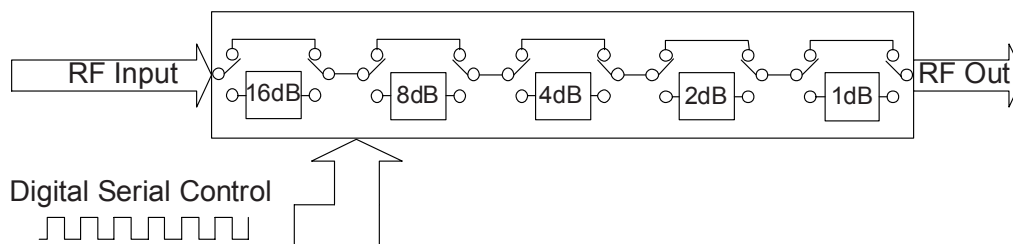
+RoHS Compliant

The +Suffix identifies RoHS Compliance. See our web site for RoHS Compliance methodologies and qualifications

General Description

The DAT-3175A-SP+ is a 75Ω RF digital step attenuator that offers an attenuation range up to 31 dB in 1.0 dB steps. The control is a 5-bit serial interface, operating on single (positive) supply voltage. The DAT-3175A-SP+ is produced using a unique CMOS process on silicon, offering the performance of GaAs, with the advantages of conventional CMOS devices.

Simplified Schematic



RF Electrical Specifications, 1-2500 MHz, $T_{AMB}=25^{\circ}C$, $V_{DD}=+3V$, 75Ω

| Parameter | Freq. Range (GHz) | Min. | Typ. | Max. | Units |
|--|-------------------|------|------------|------------|---------------|
| Accuracy @ 1 dB Attenuation Setting | 0.001-1.2 | — | 0.03 | 0.18 | dB |
| | 1.2-2.0 | — | 0.1 | 0.20 | |
| | 2.0-2.5 | — | 0.1 | 0.23 | |
| Accuracy @ 2 dB Attenuation Setting | 0.001-1.2 | — | 0.07 | 0.21 | dB |
| | 1.2-2.0 | — | 0.15 | 0.26 | |
| | 2.0-2.5 | — | 0.15 | 0.31 | |
| Accuracy @ 4 dB Attenuation Setting | 0.001-1.2 | — | 0.05 | 0.27 | dB |
| | 1.2-2.0 | — | 0.15 | 0.36 | |
| | 2.0-2.5 | — | 0.2 | 0.47 | |
| Accuracy @ 8 dB Attenuation Setting | 0.001-1.2 | — | 0.1 | 0.39 | dB |
| | 1.2-2.0 | — | 0.24 | 0.60 | |
| | 2.0-2.5 | — | 0.35 | 0.79 | |
| Accuracy @ 16 dB Attenuation Setting | 0.001-1.2 | — | 0.23 | 0.63 | dB |
| | 1.2-2.5 | — | 0.8 | 1.0 | |
| | 2.0-2.5 | — | 0.8 | 1.43 | |
| Insertion Loss ¹ @ all attenuator set to 0dB | 0.001-1.2 | — | 1.2 | 1.8 | dB |
| | 1.2-2.5 | — | 1.6 | 1.9 | |
| VSWR | 0.001-1.2 | — | 1.3 | — | :1 |
| | 1.2-2.5 | — | 1.4 | — | |
| Input IP3 (at Min. and Max. Attenuation) | .005-2.5 | — | 55-69 | — | dBm |
| Input IP2 | .005-2.5 | — | See Fig. 1 | — | dBm |
| Input Power @ 0.1dB Compression (at Min. and Max. Attenuation) | 0.030-2.5 | — | +30 | — | dBm |
| Input Operating Power | 1 MHz to 30 MHz | — | — | See Fig. 2 | dBm |
| | >30 MHz | — | — | +24 | |
| Thermal Resistance (Junction to case) | — | — | 25 | — | $^{\circ}C/W$ |

DC Electrical Specifications

| Parameter | Min. | Typ. | Max. | Units |
|-------------------------|------|------|------------------|---------|
| V_{DD} Supply Voltage | 2.3 | 3 | 3.6 ² | V |
| I_{DD} Supply Current | — | — | 200 | μA |
| Control Input Low | -0.3 | — | 0.6 ³ | V |
| Control Input High | 1.17 | — | 3.6 | V |
| Control Current | — | — | 20 | μA |

1. I. Loss values are de-embedded from test board Loss (test board's Insertion Loss: 0.10dB @ 100MHz, 0.40dB @ 1200MHz, 0.55dB @ 2000MHz, 0.75dB @ 4000MHz).
2. For operation above +3.6V see application note, AN-70-032
3. 0 Volt during power up.

Absolute Maximum Ratings⁴

| Parameter | Ratings | |
|-----------------------|------------------------------------|----------|
| Operating Temperature | -40 $^{\circ}C$ to 105 $^{\circ}C$ | |
| Storage Temperature | -65 $^{\circ}C$ to 150 $^{\circ}C$ | |
| V_{DD} | -0.3V Min., 5.5V Max. | |
| Voltage on any input | -0.3V Min., 3.6V Max. | |
| Input Power | 1-30 MHz | Figure 2 |
| | 30-2500 MHz | +30dBm |

4. Permanent damage may occur if any of these limits are exceeded.
5. Operation between max operating and absolute max input power will result in reduced reliability.

Switching Specifications

| Parameter | Min. | Typ. | Max. | Units |
|--|------|------|------|-----------|
| Switching Speed, 50% Control to 90% or 10% of RF | — | 0.4 | 0.7 | μSec |
| Switching Control Frequency | — | — | 25 | kHz |

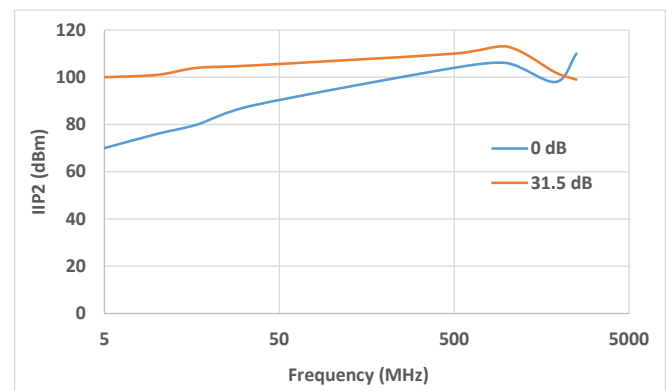
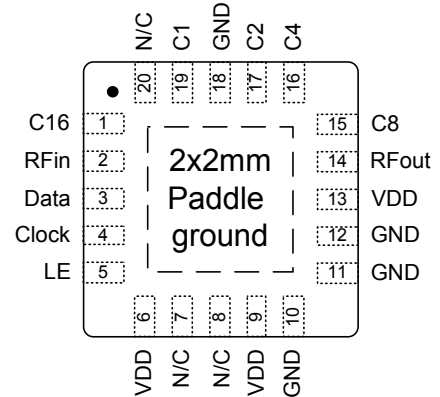


Fig 1. IP2 vs. Frequency and Attenuation

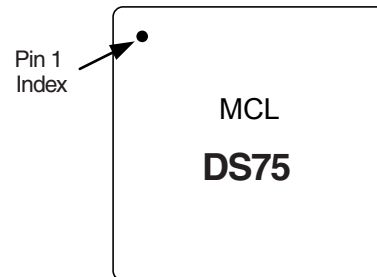
Pin Description

| Function | Pin Number | Description |
|-----------------|------------|---|
| C16 | 1 | Control for Attenuation bit, 16dB (Notes 4,7) |
| RF in | 2 | RF in port (Note 1) |
| Data | 3 | Serial Interface data input (Note 3) |
| Clock | 4 | Serial Interface clock input |
| LE | 5 | Latch Enable Input (Note 2) |
| V _{DD} | 6 | Power Supply |
| N/C | 7 | Not connected |
| N/C | 8 | Not connected |
| V _{DD} | 9 | Power Supply |
| GND | 10 | Ground connection |
| GND | 11 | Ground connection |
| GND | 12 | Ground connection (Note 7) |
| V _{DD} | 13 | Power Supply |
| RF out | 14 | RF out port (Note 1) |
| C8 | 15 | Control for attenuation bit, 8 dB (Note 4) |
| C4 | 16 | Control for attenuation bit, 4 dB (Note 4) |
| C2 | 17 | Control for attenuation bit, 2 dB (Note 4) |
| GND | 18 | Ground Connection |
| C1 | 19 | Control for attenuation bit, 1 dB (Note 4) |
| N/C | 20 | Not connected (Note 7,8) |
| GND | Paddle | Paddle ground (Note 6) |

Pin Configuration (Top View)



Device Marking



Notes:

- Both RF ports must be held at 0VDC or DC blocked with an external series capacitor.
- Latch Enable (LE) has an internal 2MΩ resistor to V_{DD}.
- Place a 10KΩ resistor in series, as close to pin as possible to avoid freq. resonance.
- Refer to Power-up Control Settings.
- The exposed solder pad on the bottom of the package (See Pin configuration) must be grounded for proper device operation.
- Ground must be less than 80 mil (0.08") from Pin 12 for proper device operation.
- This pin has internal 1MΩ pull down resistor to ground.
- Place 10KΩ resistor to ground externally.

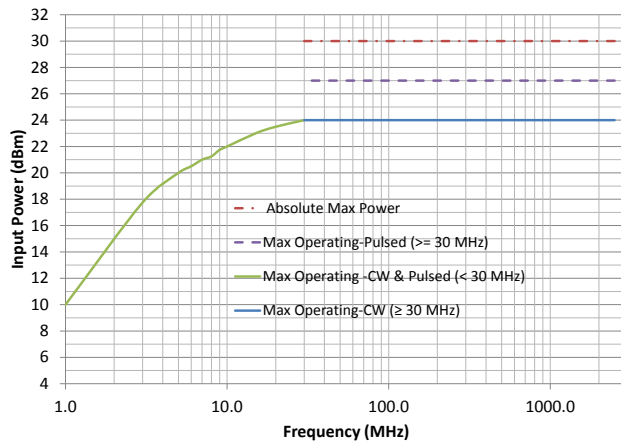
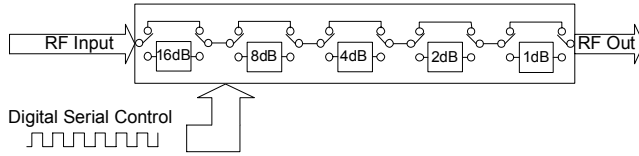


Fig 2. Max Input Power vs. Frequency.
Pulsed Power: 5% duty cycle, 4620 μs period

Simplified Schematic



The DAT-3175A-SP+ serial interface consists of 5 control bits that select the desired attenuation state, as shown in Table 1: Truth Table

| Attenuation State | C16 | C8 | C4 | C2 | C1 |
|-------------------|-----|----|----|----|----|
| Reference | 0 | 0 | 0 | 0 | 0 |
| 1 (dB) | 0 | 0 | 0 | 0 | 1 |
| 2 (dB) | 0 | 0 | 0 | 1 | 0 |
| 4 (dB) | 0 | 0 | 1 | 0 | 0 |
| 8 (dB) | 0 | 1 | 0 | 0 | 0 |
| 16 (dB) | 1 | 0 | 0 | 0 | 0 |
| 31 (dB) | 1 | 1 | 1 | 1 | 1 |

Note: Not all 32 possible combinations of C1 - C16 are shown in table

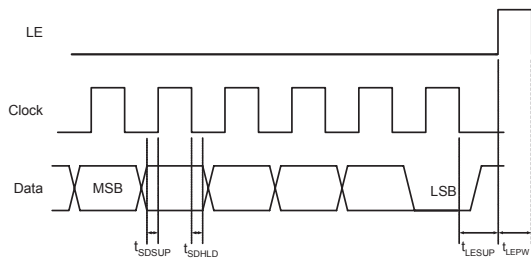
The serial interface is a 5-bit serial in, parallel-out shift register buffered by a transparent latch.

It is controlled by three CMOS-compatible signals: Data, Clock, and Latch Enable (LE). The Data and Clock inputs allow data to be serially entered into the shift register, a process that is independent of the state of the LE input.

The LE input controls the latch. When LE is HIGH, the latch is transparent and the contents of the serial shift register control the attenuator. When LE is brought LOW, data in the shift register is latched.

The shift register should be loaded while LE is held LOW to prevent the attenuator value from changing as data is entered. The LE input should then be toggled HIGH and brought LOW again, latching the new data. The timing for this operation is defined by **Figure 3** (Serial Interface Timing Diagram) and **Table 2** (Serial Interface AC Characteristics).

Figure 3: Serial Interface Timing Diagram



| Symbol | Parameter | Min. | Max. | Units |
|-------------|--|------|------|-------|
| f_{clk} | Serial data clock frequency (Note 1) | | 10 | MHz |
| t_{clkH} | Serial clock HIGH time | 30 | | ns |
| t_{clkL} | Serial clock LOW time | 30 | | ns |
| t_{LESUP} | LE set-up time after last clock falling edge | 10 | | ns |
| t_{LEPW} | LE minimum pulse width | 30 | | ns |
| t_{SDSUP} | Serial data set-up time before clock rising edge | 10 | | ns |
| t_{SDHLD} | Serial data hold time after clock falling edge | 10 | | ns |

Note 1. fclk verified during the functional pattern test. Serial programming sections of the functional pattern are clocked at 10MHz to verify fclk specification.

The DAT-3175A-SP+, uses a common 5-bit serial word format, as shown in Table 3: 5-Bit attenuator Serial Programming Register Map.

The first bit, the MSB, corresponds to the 16-dB Step and B1 bit corresponds to the 1dB step.

| B5 | B4 | B3 | B2 | B1 | B0 |
|-----|----|----|----|----|----|
| C16 | C8 | C4 | C2 | C1 | 0 |

↑
MSB
(first in)

Note: The stop bit (B0) must always be low to prevent the attenuator from entering an unknown state.

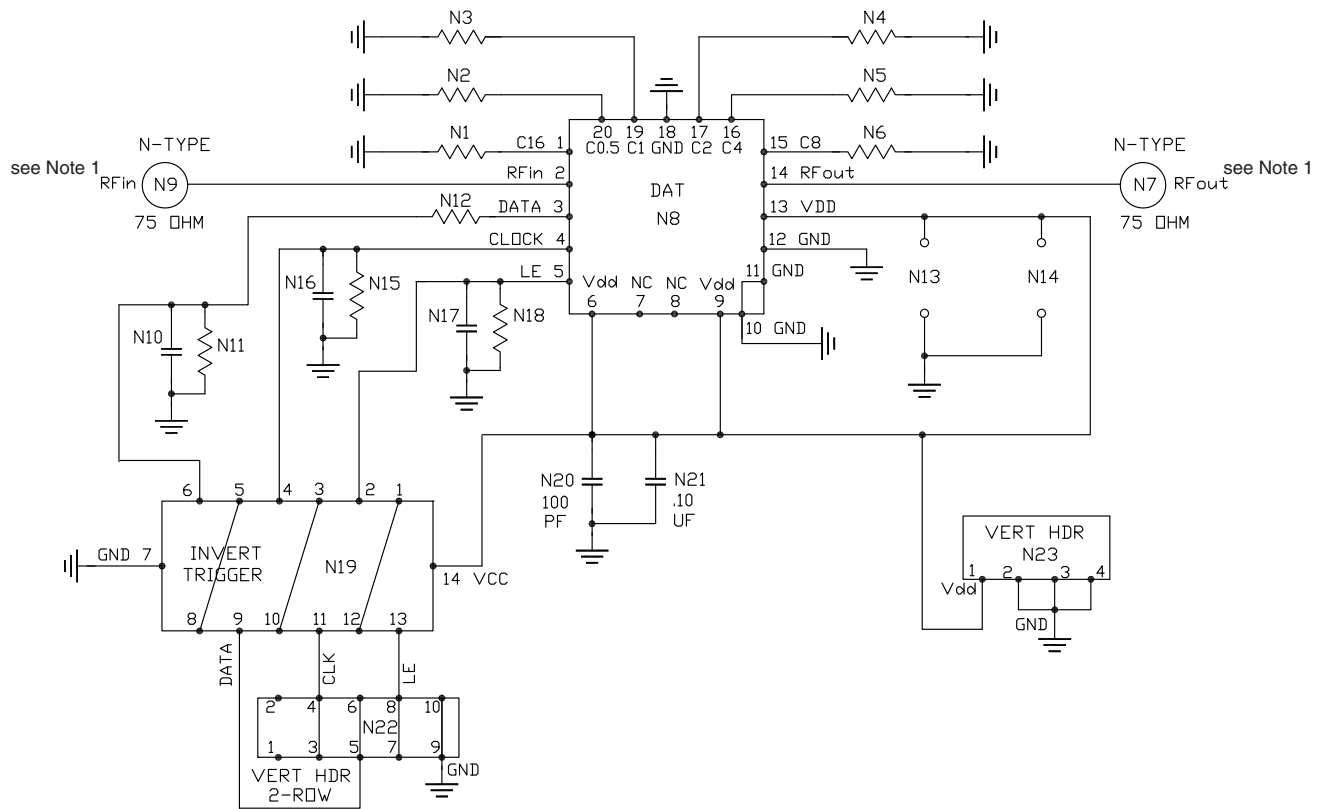
↑
LSB
(last in)

Power-up Control Settings

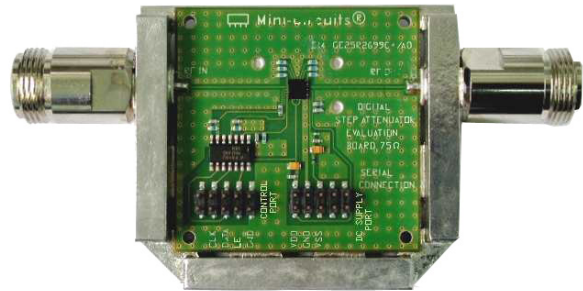
The DAT-3175A-SP+ always assumes a specifiable attenuation setting on power-up, allowing a known attenuation state to be established before an initial serial control word is provided.

When the attenuator powers up, the five control bits are set to whatever data is present on the five data inputs (C1 to C16).

This allows any one of the 32 attenuation settings to be specified as the power-up state.



Note 1: Both RF ports must be held at 0VDC or DC blocked with an external series capacitor.



TB-344

| Bill of Materials | |
|---------------------------|---------------------------------------|
| N1-N6, N11, N12, N15, N18 | Resistor 0603 10 KOhm +/- 1% |
| N10, N16, N17, N20 | NPO Capacitor 0603 100pF +/- 5% |
| N21 | Tantalum Capacitor 0805 100nF +/- 10% |
| N19 | Hex Invert Schmitt Trigger MSL1 |

** N12 can be reduced to 0Ω

| Additional Detailed Technical Information | |
|---|---|
| <i>additional information is available on our dash board. To access this information click here</i> | |
| Performance Data | Data Table |
| | Swept Graphs |
| | S-Parameter (S2P Files) Data Set (.zip file) |
| Case Style | DG983-2 <i>Plastic package, exposed paddle, lead finish: NiPdAu</i> |
| Tape & Reel Standard quantities available on reel | F87 <i>7" reels with 20, 50, 100, 200, 500 Or 1000 devices</i> <i>13" reels with 3K devices</i> |
| Suggested Layout for PCB Design | PL-203 |
| Evaluation Board | TB-344 |
| Environmental Ratings | ENV33T1 |

ESD Rating

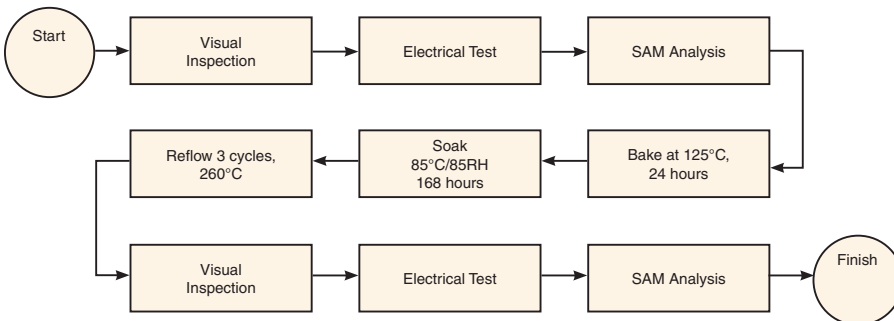
Human Body Model (HBM): Class 1C (1000 to <2000V) in accordance with MIL-STD-883 method 3015 (pass 1500V)

Charge Device Model class C2 (500 to <1000V) per JESD22-C101

MSL Rating

Moisture Sensitivity: MSL1 in accordance with IPC/JEDEC J-STD-020D

MSL Test Flow Chart



Additional Notes

- Performance and quality attributes and conditions not expressly stated in this specification document are intended to be excluded and do not form a part of this specification document.
- Electrical specifications and performance data contained in this specification document are based on Mini-Circuit's applicable established test performance criteria and measurement instructions.
- The parts covered by this specification document are subject to Mini-Circuits standard limited warranty and terms and conditions (collectively, "Standard Terms"); Purchasers of this part are entitled to the rights and benefits contained therein. For a full statement of the Standard Terms and the exclusive rights and remedies thereunder, please visit Mini-Circuits' website at www.minicircuits.com/MCLStore/terms.jsp